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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/538,458	06/10/2005	Lonnie Goff	US02 0598 US	3872

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EXAMINER	
MAMO, ELIAS	

ART UNIT	PAPER NUMBER
2184	

NOTIFICATION DATE	DELIVERY MODE
09/07/2007	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

ip.department.us@nxp.com

Office Action Summary	Application No.	Applicant(s)	
	10/538,458	GOFF, LONNIE	
	Examiner	Art Unit	
	Elias Mamo	2184	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 June 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *06/10/2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-10 are rejected under 35 U.S.C. 102(b) as being anticipated by Martel et al. (US 5,887,165), herein after referred to as Martel et al. '165.

Referring to **claim 1**, Martel et al. '165 teach, as claimed, a method of performing configuration or control of a subsystem (i.e.-method for a dynamically reconfiguring hardware system, col. 2 line 4), comprising: providing together with the subsystem a configuration/control unit (i.e.-reconfigurable hardware system, col. 2, line 4) having a controller portion (controller, col. 2, line 6) and a storage portion storing configuration parameters (i.e.-configuration memory 19, see fig. 1 and col. 2, line 5-6); the configuration/control unit receiving an activation signal (i.e.-configuration signal, col. 2, line 14); and the configuration/control unit, in response to the activation signal, performing configuration or control of the subsystem, including storing at least one configuration parameter at a location within the subsystem (col. 2, lines 52-53).
As to **claim 2,** Martel et al. '165 teach the method of claim 1 wherein the subsystem is a hardware subsystem (col. 3, line 39), and the configuration/control unit is a hardware configuration/control unit (i.e.-processor 17, col. 3, lines 43 and 49).

As to **claim 3,** Martel et al. '165 inherently teach the method of claim 1 wherein the hardware subsystem and the hardware configuration/control unit are provided together within the same integrated circuit (i.e.-system 11, col. 3, line 39).

As to **claim 4,** Martel et al. '165 teach the method of claim 1 wherein the activation signal is a configuration/control ID (col. 2, line 1).

As to **claim 5,** Martel et al. '165 teach the method of claim 4 wherein the configuration/control unit is responsive to multiple different configuration/control IDs for performing different corresponding configuration or control actions with respect to the subsystem (col. 2, lines 12-16).

Referring to **claim 6,** Martel et al. '165 teach, as claimed, a subsystem having self-configuration capabilities, comprising: a register section including multiple registers (i.e.-reconfigurable logic module, col. 2, lines 23-24), the subsystem functioning differently depending on contents of the registers; and a configuration/control unit (i.e.-reconfigurable hardware system, col. 2, line 4) having a controller portion (i.e.-controller, col. 2, line 6) and a storage portion storing configuration parameters (i.e.-configuration memory 19, col. 2, lines 5-6 and fig. 1); wherein the configuration/control unit is responsive to an activation signal for performing configuration or control of the subsystem (col. 2, lines 12-14), including storing at least one configuration parameter at a location within the subsystem.

As to **claim 7,** Martel et al. '165 teach the apparatus of claim 6 wherein subsystem is a hardware subsystem (reconfigurable hardware system 11, se fig. 1 and col. 3, line 39), and the configuration/control unit is a hardware configuration/control unit (i.e.-CPU 17, see fig. 1 and col. 3, lines 43 and 49).

As to **claim 8,** Martel et al. '165 inherently teach the apparatus of claim 7 wherein the hardware subsystem and the hardware configuration/control unit are provided together within the same integrated circuit (i.e.-system 11, col. 3, line 39).

As to **claim 9,** Martel et al. '165 inherently teach the apparatus of claim 6 wherein the activation signal is a configuration/control ID (i.e.-configuration signal, col. 2, line 14).

As to **claim 10,** Martel et al. '165 teach the apparatus of claim 9 wherein the configuration/ control unit is responsive to multiple different configuration/control IDs for performing different corresponding configuration or control actions with respect to the subsystem (col. 2, lines 12-16).

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

- Madurawe (US 7,064,579) teaches alterable application specific integrated circuit;
- Ptasinski et al. (US 6,363,437) teach plug and play I^2C slave; and
- Takahashi et al. (US 5,887,193) teach system for loading control information from peripheral devices to a controller in response to connection operation.

Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Elias Mamo whose telephone number is (571) 270-1726 and fax number (571) 270-2726. The examiner can normally be reached on Monday to Thursday from 9 AM to 5 PM EST. The examiner can also be reached on alternate Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, DR. Henry Tsai, can be reached on (571) 272-4176. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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HENRY TSAI
SUPERVISORY PATENT EXAMINER

8/31/07